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The WBS-VIII FFT-Based Spectrometer and Instrument Interfacing with SpaceFibre

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***Abstract*— SpaceFibre [1] is a high-performance, high-reliability and high-availability network technology designed for demanding applications. The WBS-VIII is the latest generation of FFT-based spectrometer being developed by STAR-Dundee for in-orbit microwave sounder applications. This paper describes the architecture of the WBS-VIII, outlines its development and expected performance, and then explains why SpaceFibre was used as the interface between the WBS-VIII and the Instrument Control Computer.**

Keywords—SpaceFibre, Payload Data-Handling, Serial Communications, Networks, Spectrometer, Instrument

I. INTRODUCTION

SpaceFibre [1] is a data link and network technology developed specifically for spacecraft on-board data-handling. It runs over electrical or fibre-optic cables, operates at very high data rates, and provides in-built quality of service, and fault detection, isolation and recovery capabilities. Because of these important characteristics, SpaceFibre is now flying in several spacecraft and being designed into over 60 more.

For instruments which have a modest data rate e.g. 200 Mbit/s, SpaceWire [2] may seem to be the obvious choice for collecting the data from them, but the capabilities of SpaceFibre make it very attractive for interfacing to moderate (100 Mbit/s), high (1 Gbit/s), very high (10 Gbit/s) and extremely high data-rate instruments.

This paper describes a moderate data rate instrument and then explains why SpaceFibre was used as its data and control interface. Some of the facilities inherent in SpaceFibre beyond the raw performance, are used to significant advantage.

II. THE SPECTROMETER INSTRUMENT

The WBS-VIII is a wideband spectrometer (WBS) which is being developed to fly on the Hyperspectral Microwave Sounder (HyMS) In-Orbit Demonstrator (IOD) being developed by Spire. WBS-VIII is the data processing backend of the microwave instrument. It is an 8-channel FFT-based spectrum analyser, the eighth spectrometer that STAR-Dundee has been involved in and the seventh one that STAR-Dundee has designed.

Each channel in the WBS-VIII is sampled by an ADC at 5 Gsamples/s giving a bandwidth of around 2.2 GHz taking anti-aliasing filter roll-off into account. Each channel is then processed by an FFT to give 2048-point real spectra and a corresponding FFT bin width of 1.22 MHz. The WBS-VIII spectrometer is based around the AMD RFSoC FPGA device.

The acquired spectra are accumulated within the WBS-VIII over a programmable integration time. The resulting spectra are sent to an Instrument Control Computer (ICU) over a SpaceFibre link. The SpaceFibre interface is also used to configure, control and monitor the WBS-VIII. The ICU sends trigger broadcast messages to the WBS-VIII to control the timing of data acquisition which is synchronised to the position of the instrument antenna.

The integration extracts the microwave spectra from the background noise and reduces the data rate by a factor of around 10,000. So, despite the huge volume of data entering the WBS-VIII, the data rate coming out is modest.

The WBS-VIII system architecture is illustrated in Figure 1.

A. RF Inputs

There are eight RF inputs to the WBS-VIII. Each input is a real signal of 2.5 GHz bandwidth. The sample rate of each ADC is 5 Gsamples/s enabling a signal up to a possible bandwidth of 2.5 GHz to be processed. Anti-aliasing filters are external to the WBS-VIII.

The RF input to each ADC is passed through an RF switch, which is used to isolate an active RF input signal from the ADC input when the WBS-VIII is powered down. The RFSoC can be damaged if an RF signal is applied to the ADC input when the RFSoC is not powered. It is also necessary to isolate the RF inputs from the ADC inputs for a short period of time after the RFSoC is powered up to allow the ADCs to be calibrated, which is carried out automatically by the RFSoC. The RF switch provides the necessary isolation of the ADC inputs.

The RF input is a 50-ohm single-ended signal and the RFSoC ADCs have 100-ohm differential inputs. The output of the RF switch is passed through a balun which converts the 50-ohm single-ended (unbalanced) input signal to a 100-ohm differential (balanced) signal for the ADC inputs.

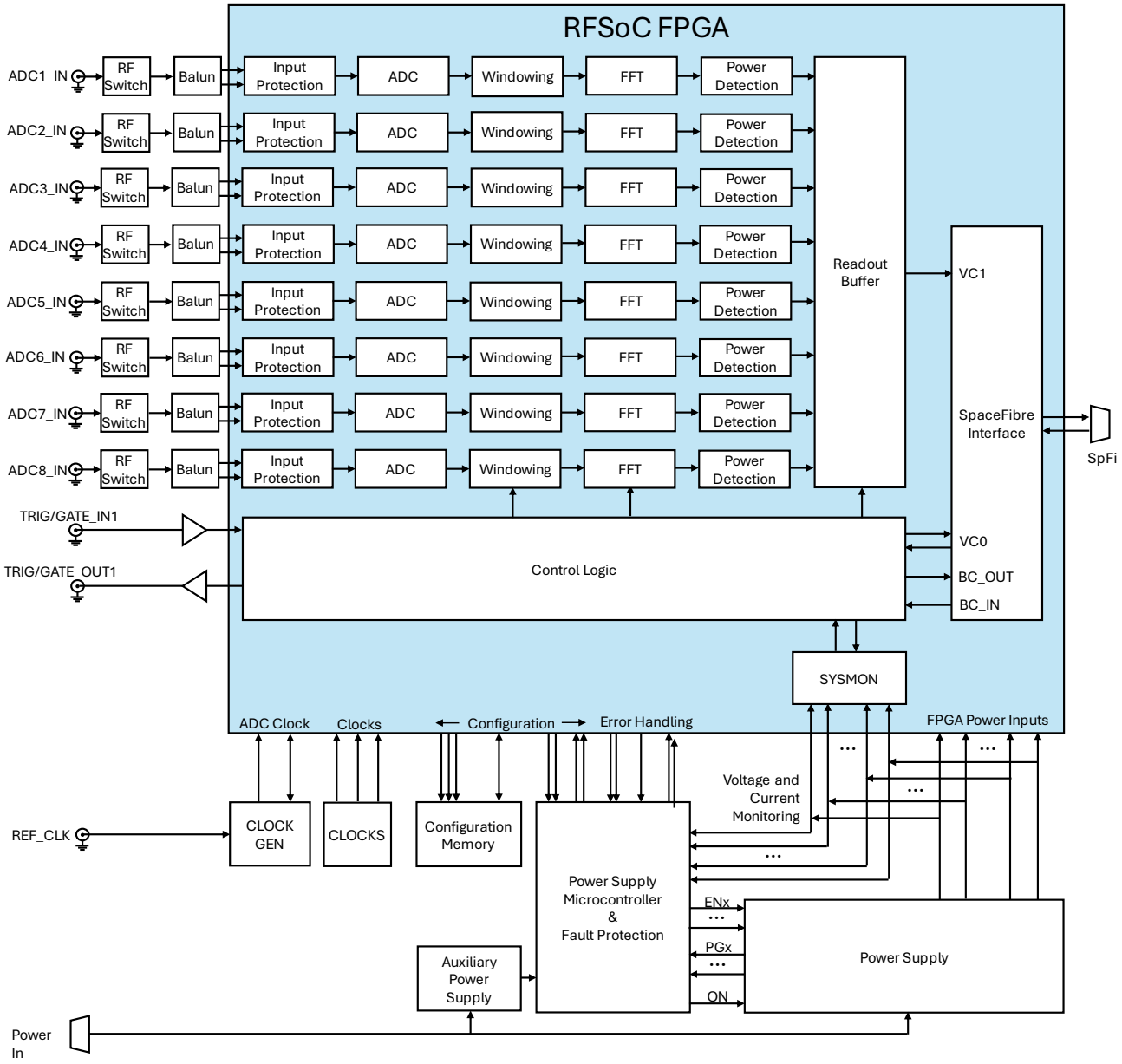

Figure 1: WBS-VIII System Architecture

The RF inputs are sensitive to clock breakthrough, noise on the power rails and cross-talk. The layout of the WBS-VIII PCB and the arrangement of the housing aim to mitigate these potential issues.

B. FFT Processor

The FFT processor is implemented in the FPGA fabric of the RFSoC device. Eight FFT channels are provided in the RFSoC. Each FFT channel takes the real data from an ADCs and processes it with a FFT to produce the spectra of the input signal. Programmable windowing, power detection and programmable integration time capabilities are provided. Integrated spectra of 2048 spectral samples from each input channel are placed in a read-out buffer and transferred over SpaceFibre to the instrument control unit.

C. ADC Clock Generation

The ADCs operate with a sample clock of 5 Gsamples/s. It is required for the ADC sample clock to be phase locked to an ultra-stable reference clock. A 50 MHz external reference clock is multiplied up to 400 MHz using a phase-locked loop and voltage-controlled crystal oscillator (VCXO). The 400 MHz clock is provided to the RFSoC, which is then divided and multiplied inside the RFSoC to give the ADC sample rate of 5 Gsamples/s.

The 400 MHz synchronised clock is provided by a clock management chip which incorporates the phase-locked loop and clock dividers, and is programmable over an SPI interface. The VCXO is programmable over an I2C interface to the required nominal 400 MHz centre frequency.

When the WBS-VIII powers up, the RFSoC is configured from configuration memory. The RFSoC then configures the VCXO and clock manager, configures and calibrates the ADCs, and then is ready for operation.

D. Configuration

The RFSoC FPGA and processor system is configured and booted from a radiation-tolerant, non-volatile memory. Configuration of the RFSoC is carried out over a Quad SPI interface. On power-up, once all the power supplies are stable, the power supply micro controller indicates to the RFSoC that it can start configuration. The RFSoC then pulls the configuration data from the configuration memory device and programs the internal FPGA configuration memory.

E. Power Supply

The power supply provides each of the power rails required by the RFSoC and the other WBS-VIII circuitry. The input power is unregulated in the range 6.8 to 8.2 Volts. This is passed to an auxiliary power supply, which provides 3.3 V to the power supply microcontroller and fault detection circuitry, and to a power switch (eFuse) that feeds the point-of-load (POL) converters for each power rail. The POLs are arranged in five groups so they can be powered up in sequence to avoid excessive inrush current. The power supply was designed using Texas Instruments radiation tolerant components.

F. Power Supply Microcontroller

The power supply microcontroller is responsible for controlling the power supply. When power is applied to the WBS-VIII the power supply microcontroller powers up and checks the input power voltage. When the input voltage is at an acceptable level, the power supply microcontroller turns on the power switch (eFuse) and then enables each POL group in sequence. When all the POL groups are at their operational voltage, the power supply microcontroller instructs the RFSoC to begin configuration. After RFSoC configuration the power supply microcontroller monitors the voltages of the power rails, the currents flowing and various fault signals from the RFSoC. When the input power is removed or if any fault occurs, the power supply microcontroller switches off power to the POLs.

G. SysMon

The system monitor (SysMon) function inside the RFSoC is a multi-channel ADC and controller which can be used to measure power rail voltages, current flow and the temperature of the RFSoC. The measurements are stored in registers in the RFSoC and can be accessed via the Remote Memory Access Protocol (RMAP) over VC0 of the SpaceFibre interface. This allows the instrument control unit (ICU) to read detailed status information from the WBS-VIII.

H. Fault Protection

A set of over-voltage comparators are used to monitor the principal voltage rails. Any over-voltage condition will result in power being cut by immediately switching off the power switch and discharging the power rails to the RFSoC.

The power rail voltages and currents are read by an ADC in the power supply microcontroller and checked for undervoltage conditions.

The RFSoC PSLP (low-power processing system) monitors the state of the configuration memory and raises an error flag if an SEU error is detected in the configuration memory. This error signal causes the power supply microcontroller to power cycle the WBS-VIII POLs and to reconfigure the RFSoC, recovering from the SEU induced error. The RFSoC also provides heartbeat signals to the power supply microcontroller for fault detection; a missed heartbeat also resulting in power cycling of the WBS-VIII POLs.

If a fault persists and is not cleared by power cycling the WBS-VIII POLs, the power supply microcontroller will continue to try to recover from the fault by repeated power cycling. This is stopped only when the power input to the WBS-VIII is removed. The power supply micro controller will shut down the POLs and then remain off. Switching off the power input to the WBS-VIII, waiting for several seconds, and then switching on power again might possibly remove a persistent fault.

When the WBS-VIII POLs are powered down, the ADC inputs are isolated by the RF switches, the Reference Clock input is isolated, and the trigger input and output are cold sparing.

III. Spectrometer Implementation

The WBS-VIII is being implemented for flight on an in-orbit demonstrator. The components used are suitable for use in low Earth orbit with an appropriate level of radiation shielding. The ADCs and FFT processors are implemented in an AMD RFSoC FPGA device using VHDL.

A. Simulation of the FFT Processor

The FFT processor design was simulated in software to ensure that the design would provide an appropriate level of performance. The simulation results are shown in Figure 2.

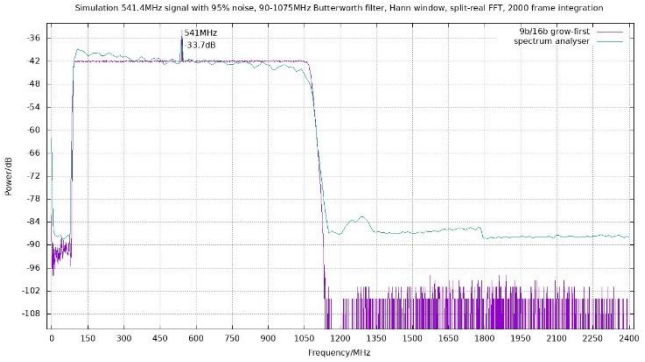

Figure 2: WBS-VIII Simulation Performance (Purple) versus a Spectrum Analyser (Green)

The simulated test signal comprises a single-frequency tone at 541 MHz, added to a broadband signal in the range 90-1075 MHz. The computed spectrum is the purple trace in Figure 2. The green trace is a real signal with the same characteristics fed into a laboratory test equipment spectrum analyser for general comparison. Overall the WBS-VIII design performed well.

B. Breadboard Implementation of FFT Processor

The WBS-VIII was then implemented in VHDL and tested on a commercial development board for the RFSoC FPGA. The test system is shown in Figure 3. A signal generator is used to provide the 541 MHz tone and a broadband white noise generator used to provide the broadband noise signal, which was bandlimited to 90-1075 MHz by a filter. The

resulting test signal is then passed into one channel of the WBS-VIII at a time.

The results are shown in Figure 4. The spectrum measured by the WBS-VIII is the purple trace. A spectrum analyser, which is on the top of the set of test equipment in Figure 3, was used to measure the spectrum of the test signal for comparison with the WBS-VIII (green trace).

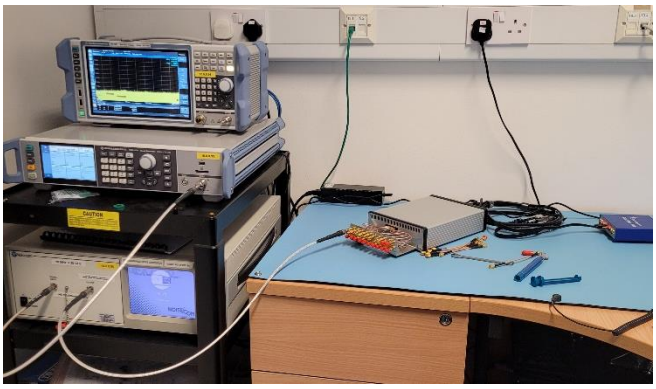

Figure 3: WBS-VIII Breadboard Under Test

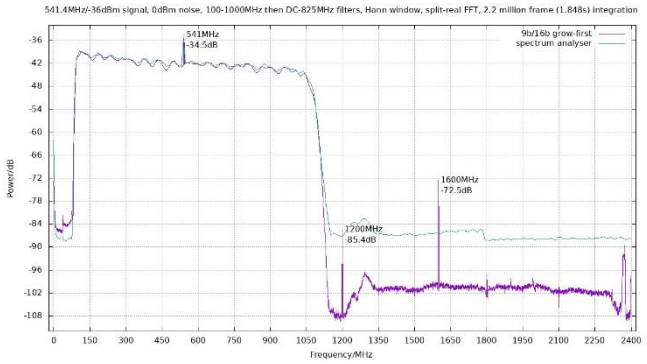

Figure 4: WBS-VIII Breadboard Performance (Purple) versus a Spectrum Analyser (Green)

The WBS-VIII results match the spectrum analyser measurement closely, with two areas of departure:

- The noise floor of the WBS-VIII is lower than that of the spectrum analyser.
- The WBS-VIII shows some clock breakthrough at 1200 and 1600 MHz and possibly close to 2400 MHz.

The clock breakthrough is unwelcome, although it would be largely calibrated out by the sounder instrument calibration routine, so great care was taken in the WBS-VIII board and enclosure design to prevent clock breakthrough and crosstalk between channels.

C. Electronics Development

The design of the electronics for the WBS-VIII is complete, the board has been manufactured and is being tested. A CAD model of the PCB is shown in Figure 5.

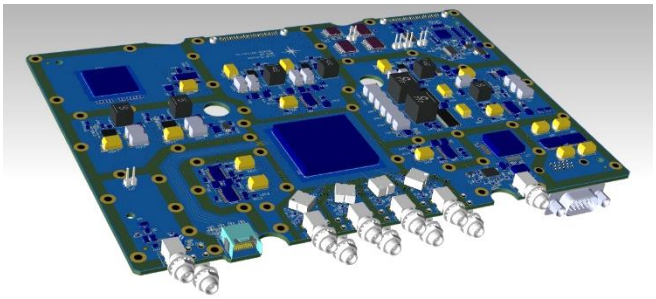

Figure 5: CAD Model of the WBS-VIII PCB

D. Enclosure Design

The enclosure for the WBS-VIII has been designed with four purposes in mind:

- To support the PCB to ensure that shock and vibration requirements are met.
- To provide a thermal path from the FPGA and other power hungry components to the baseplate of the WBS-VIII which is a cold surface.
- To electrically shield the sensitive parts of the circuitry from the noisier parts, specifically countering clock breakthrough and channel-to-channel crosstalk. Also, to ensure that the EMC requirements for the WBS-VIII are met.
- To act as a radiation shield to increase the resilience against total ionising does radiation.

A CAD model of the WBS-VIII enclosure is shown in Figure 6. The WBS-VIII provides a short distance from the heat sources to the baseplate. The WBS-VIII is mounted on the baseplate using bolts around the perimeter of the unit and also two bolts in the middle. This improves structural integrity and ensures good thermal contact with the cold surface below the WBS-VIII.

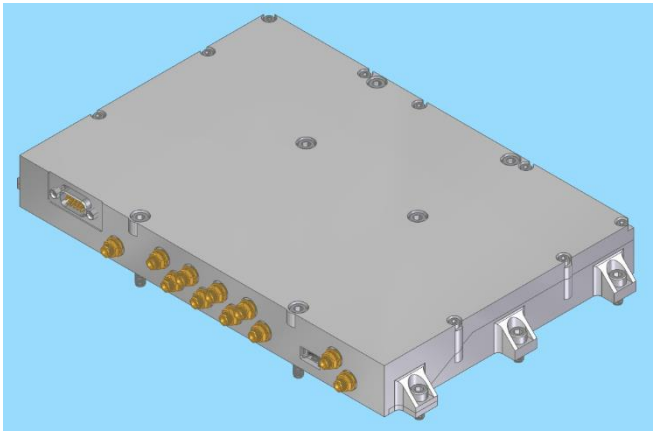

Figure 6: CAD Model of the WBS-VIII Enclosure

The connectors on the front panel are, from left to right:

- High density D-Sub (15-way) power connector, which is wired according to the draft Space Power Consortium standard.

- SMA reference clock input, providing a 50 MHz ultra-stable clock signal to which the ADC sample clock is phase synchronised.
- Eight SMA RF signal input connectors, one for each channel of the WBS-VIII.
- A Samtec ARF6 connector for the SpaceFibre interface.
- Two SMA connectors for hardware trigger in and trigger out.

IV. SpaceFibre in the WBS-VIII

A. SpaceFibre Key Features

The key features of SpaceFibre are outlined below:

- Very high-performance, with 3.125 Gbit/s single-lane performance (including overhead for 8B/10B encoding) in the Microsemi RTG4, giving 12.5 Gbit/s with four lanes, and 6.25 Gbit/s per lane in Xilinx XQRKU060 and Microchip PolarFire, giving 25 Gbit/s with four lanes.
- Electrical and Fibre Optic media with the electrical medium supporting cable lengths up to 5m, depending on data rate, and fibre optics supporting up to 100m.
- High reliability and high availability using error-handling technology which is able to recover automatically from transient errors in a few microseconds without loss of information and which is able to continue operation, preserving transfer of critical and important information when a lane in a multi-lane link fails.
- Multi-lane capability providing increased bandwidth aggregated into an overall link bandwidth, rapid (few μs) graceful degradation in the event of a lane failure, hot and cold lane redundancy, and support for asymmetric traffic with unidirectional lanes.
- Quality of service using multiple virtual channels across a data link, each of which is provided with a priority level, a bandwidth allocation and a schedule.
- Virtual networks that provide multiple independent traffic flows on a single physical network, which, when mapped to a virtual channel, acquire the quality of service of that virtual channel.
- Deterministic data delivery of information using the scheduled quality of service, in conjunction with priority and bandwidth allocation.
- Low-latency broadcast messages which provide time-distribution, synchronisation, event signalling, error reporting and network control capabilities.
- Small footprint which enables a complete SpaceFibre interface to be implemented in a radiation tolerant FPGA, for example, around 3% of an RTG4 FPGA for a typical instrument interface with two virtual channels.
- Backwards compatibility with SpaceWire at the network level, which allows simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.
- SpaceFibre is a data and control plane technology in the revised VITA 78 standard (SpaceVPX-2022) and a data-plane technology in the ADHA standard.

B. SpaceFibre in the WBS-VIII

SpaceFibre is normally used to provide high data-rate interconnect. The data-rate of the WBS-VIII is well within the capabilities of a SpaceWire interface, so why was SpaceFibre used? There are several reasons which are considered in the following subsections:

1) Availability of SerDes (MGT) on the RFSoC FPGA

Many FPGAs now include Serialisers/Deserialisers (SerDes), otherwise known as Multi-Gigabit Transceivers (MGTs). This makes the inclusion of SpaceFibre in a device possible. The cost is the additional power supplies required to power the MGTs.

2) Low Power of the MGTs

When MGTs were implemented in external devices to the FPGA using devices such as the TLK2711, the power consumption per lane was very high. That is no longer the case. MGTs embedded in recent FPGAs have very low power consumption.

C. Low Mass, Flexible Cable

The mass of the SpaceFibre electrical cable is much less than that of a SpaceWire cable (around half the mass) and the SpaceFibre cable is much more flexible. This simplifies cable routing and makes routing of cables through tight spaces possible.

D. Broadcast Messages

Broadcast messages are short, low-latency messages that are broadcast across a SpaceFibre network.

Broadcast messages can also go from the WBS-VIII to the ICU (or other parts of a system). Each broadcast message has the following fields:

- Broadcast Channel: this is normally the logical address of the unit sending the broadcast message. It is used to identify the source of the broadcast message.
- Broadcast Type: the type of information that the broadcast message is carrying. For example this could be Time Type, which means that the User Data field is carrying a CCSDS unsegmented time-code. The Time type of broadcast message is used for distributing system time information to all nodes in a network that need to know the time.
- User Data: 8-bytes of user information carried in the broadcast message, which is defined by the Broadcast Type.

The Broadcast Types that the WBS-VIII uses are:

- Trigger
- Status
- Emergency

E. Broadcast Triggering

It is necessary to synchronise the capture of data by the WBS-VIII with the position of the antenna. To do this the ICU has to provide a trigger to the WBS-VIII, upon receipt of which the WBS-VIII will start capturing data. This is not a high precision trigger, and something in the region of 10 µs is adequate. External hardware trigger-in and trigger-out connectors are provided on the WBS-VIII for this purpose.

It is, however, possible to provide the triggering function using a SpaceFibre broadcast message. The ICU simply sends a broadcast message to the WBS-VIII and the WBS-VIII starts data capture when it reads it. The possible problem is the time it takes for the ICU software to set up and for the broadcast message to be sent. However, SpaceFibre broadcast messages have been designed with low latency in mind. To send a broadcast message the ICU has simply to write to a register. The broadcast message is then sent very quickly. It takes less than 1 µs from the ICU writing to the register for the WBS-VIII to be acting on it.

When triggered, the WBS takes several measurements of the atmosphere, one after the other, each forming a pixel of atmospheric data. For each pixel of data, spectra are computed and integrated, until the antenna is pointing at the next pixel. There are also two calibration positions of the antenna, where calibration pixels are acquired.

The ICU needs to tell the WBS-VIII how many pixels need to be acquired for each scan. This can be done by an RMAP write over SpaceFibre to registers in the WBS-VIII, but that takes some time and requires further synchronisation. The broadcast message can carry eight bytes of user information, which can in the WBS-VIII define how many pixels to acquire and where the antenna will be pointing (atmosphere or a calibration target). That information is available immediately in registers when the broadcast message arrives. The ICU writes the information to a register and the broadcast message is sent carrying that information. The writing to one or two registers is all that the ICU needs to do, to trigger acquisition of the required amount of data and to provide meta-data to be attached to the integrated spectra sent back from the WBS-VIII to the ICU.

Not only is the hardware simplified, there is no need for the trigger cables which might need to be cross-strapped for redundancy purposes, but the ICU software is simplified too. The whole system is more responsive, more flexible, and more dynamic (allowing fast changes to the trigger parameters).

F. Broadcast Status

The ICU needs to keep track of the status of the WBS-VIII, monitoring its activity, temperature, voltage rails, and power consumption. This can be done with one or more RMAP reads.

An alternative is to send a broadcast message periodically from the WBS-VIII to the ICU carrying the most important status information, e.g. power good flags, temperature alert, current pixel number, scan finished, etc.

Sent every 0.1 ms to the ICU, the Status broadcast message provides an easy way for the ICU software to see the status of the WBS-VIII. The status broadcast messages can be sent automatically. When received at the ICU the SpaceFibre interface puts the status information in a register, where it can be accessed at the convenience of the ICU software. The software will be able to read the latest status information which is no more than 0.1 ms old. The link bandwidth used to continually send a status broadcast message is insignificant: <0.0001% at a link speed of 3.1225 Gbit/s.

RMAP read commands can be used less frequently, if required, to gather further housekeeping information.

G. Emergency Broadcast

If a critical fault or SEU occurs in the WBS-VIII, the response is to power cycle the majority of the WBS-VIII components, with the exception of the power supply control circuitry. It will take a couple of seconds from the fault occurring to operation of the WBS-VIII being restored (assuming the fault is a transitory fault). From the ICU's perspective the WBS-VIII will cease sending data, or responding to commands, and the SpaceFibre link will be disconnected. It would be helpful for the ICU to know that this is going to happen, rather than having to figure it out from the symptoms.

The low latency of the broadcast message can help. When a critical fault occurs an Emergency broadcast message can be sent to indicate that the WBS-VIII will be power cycling. If the fault is caused by an overvoltage condition, possibly as a result of an SEU in a point-of-load converter, it is essential to power down quickly to prevent any damage. The speed with which the broadcast message can be sent enables the message to be transmitted before power is lost. The ICU will then know why the WBS-VIII is not responding.

V. Conclusions

SpaceFibre has been used as the interface to an instrument processor unit, the WBS-VIII, which does not need the high data-rates that SpaceFibre provides. This paper has explained why. The many capabilities of SpaceFibre enable it to provide services that would not normally be thought of, which not only reduce hardware complexity, but also simplify the software in the ICU controlling the instrument processing unit.

The WBS-VIII is currently being tested in preparation for flight.

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