A SpaceFibre Routing Switch for Distributed Payload Processing and Backplane Interconnect

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***Abstract*—SpaceFibre [1] is now operating in space and being designed into many more space missions. This paper considers a critical element in a SpaceFibre network, the routing switch, and describes an implementation which has been developed to technology readiness level (TRL) 5/6.**

Keywords—SpaceFibre, On-board Data Handling, Networks, ADHA, SpaceVPX, VNX+

I. Introduction

SpaceFibre is a data-link and network technology which is designed for spacecraft and other demanding applications. SpaceFibre can be used in a fully distributed architecture or as an interconnect between boards in a rack. This paper introduces SpaceFibre and then describes the Hi-SIDE project [2], which developed a "Flat-Sat" to demonstrate a distributed payload data-handling network based on SpaceFibre. A critical element of a SpaceFibre network is the SpaceFibre routing switch. The application requirements for the routing switch are summarised, the Hi-SIDE demonstration system outlined, the STAR-Tiger SpaceFibre routing switch described, and the results of the Hi-SIDE project, demonstrating the SpaceFibre distributed architecture, are summarised. Three different standards for data-handling and processing units are then described briefly, where SpaceFibre is either the primary, or one of a couple of possible, high-speed data-link and network technologies that are supported by those standards.

II. SpaceFibre

SpaceFibre is a high-performance, high-reliability and high-availability data-link and network technology suitable for spacecraft payload data-handling and other demanding applications. SpaceFibre can operate over electrical or fibre optic media. Each lane can operate at data rates of 6.25 Gbit/s, with higher data rates also possible depending on the serialiser/deserialiser (SerDes) technology available. Multiple lanes provide higher data rates; for example, a quad-lane link gives 25 Gbit/s (19.2 Gbit/s user data rate). Links can have hot or cold redundant lanes, and be asymmetric with more lanes in one direction than in the other. SpaceFibre supports quality of service (QoS) using virtual channels to carry different classes of traffic. Each virtual channel (VC) can be assigned a priority, an allocated bandwidth and a schedule. These three attributes work together to ensure that traffic flowing on one VC cannot adversely affect traffic flowing on another VC. They behave like independent links, which run over the same physical link. Different QoS attributes can be applied in each direction of a link. The schedule attribute is used to support deterministic data delivery for applications such as attitude and orbit control systems, enabling a single network to be used for both spacecraft control and payload data-handling. SpaceFibre also provides a broadcast mechanism which can broadcast short messages that carry 8-bytes of user information together with broadcast channel and broadcast type information. Broadcast messages can be used to distribute system time, to perform equipment synchronisation, to signal events or system errors, etc.

SpaceFibre links can be connected directly between electronic units or from a unit to a SpaceFibre routing switch. The SpaceFibre routing switch transfers packets from one port to another port according to the address on the packet. Each virtual channel of a link is assigned to a virtual network inside a routing switch. Information from one virtual network cannot cross to another virtual network. The virtual networks behave as separate logical networks which adhere to the QoS settings of the virtual channels that have been mapped to them.

SpaceFibre is compatible with SpaceWire at the network level, sharing the same packet format and addressing scheme. This makes it easy to connect SpaceWire devices into a SpaceFibre network.

STAR-Dundee provides a comprehensive range of SpaceFibre IP cores including Single- and Multi-Lane Interfaces and Single- and Multi-Lane routing switches. Other IP cores that support efficient processor to processor communication are currently under development.

STAR-Dundee SpaceFibre IP cores are flying in at least two operational Earth Observation missions, and are being designed into many other important European and USA satellites. STAR-Dundee SpaceFibre IP cores are available for a wide range of FPGAs, including Microchip RTG4 and RT PolarFire and Xilinx KU060 and Versal FPGAs, with support for NanoXplore and Lattice/FrontGrade FPGAs currently under development.

III. Hi-SIDE Project

The Hi-SIDE project is a European Union project carried out by several leading aerospace organisations from across Europe. The Hi-SIDE project has developed critical satellite data-chain technologies for handling and transferring data from instruments to processing and storage elements on-board the spacecraft, and to the downlink transmitters that send data to ground. The Hi-SIDE project culminated in a comprehensive demonstration incorporating all the critical elements of the High-Speed Data Chain (HSDC) from instrument to ground-station. The Hi-SIDE project was presented with the Innovation in Space Award from the European Space Forum in 2022.

The SpaceFibre network developed for Hi-SIDE will be used in subsequent sections as an example of a SpaceFibre network that interconnects a set of discrete payload data-handling elements on board a spacecraft.

IV. Router Requirements For Hi-SIDE

The Hi-SIDE payload data-handling architecture was fully distributed with several instruments, payload data-handling units and downlink transmitters connected together using a SpaceFibre routing switch. The following units were interconnected forming a demonstration system representative of an Earth observation mission with demanding on-board data rates. The organisations that developed the various units are indicated in parentheses.

- Camera providing real-time images at a data rate of around 4.6 Gbit/s (STAR-Dundee).
- Instrument simulator providing hyperspectral data (or other forms of data) at a data rate of around 9 Gbit/s (STAR-Dundee).
- Mass-memory simulator [3] implemented in a PC with SpaceFibre interface. Data rates into the mass-memory of up to 14 Gbit/s are possible (STAR-Dundee).
- Control Computer (PC-based) [3] which is used to configure, control and monitor the SpaceFibre network and equipment connected to the network (STAR-Dundee).
- Data compressor [4] which performs CCSDS 123.0-B-2 Low-Complexity Lossless and Near-Lossless Multispectral and Hyperspectral Image Compression at data rates of around 7.5 Gbit/s (Airbus and NKUA).
- Low power consumption High-Performance Data Processor (HPDP) [5] which was programmed to perform data encryption (ISD).
- Radio Frequency (RF) downlink [6] (TESAT designing the modulator, ERZIA developing an RF power amplifier and Kongsberg developing a demodulator).
- Optical downlink simulator - an image viewer which replaced the optical downlink [7] in the final demonstration. The 10 Gbit/s optical downlink was demonstrated separately due to component availability issues. (DLR)
- File Protection Scheme (FPS) [8] for protecting data from gaps in the optical data stream caused by atmospheric effects. In the demonstration, the FPS encoder was run on the mass-memory PC and the FPS decoder was run on a dedicated PC connected to the SpaceFibre network – normally this would be performed on ground. (DLR)

The camera, data compressor, HPDP, RF downlink and optical downlink all incorporated the STAR-Dundee Multi-Lane SpaceFibre interface IP core so they could connect to the SpaceFibre network. Various types of FPGA were used on the different units. The instrument simulator, mass-memory simulator and control computer used the STAR-Dundee STAR-Ultra PCIe board which provides a high-speed interface between SpaceFibre and a host PC.

The STAR-Tiger SpaceFibre routing switch is the primary element of the payload data-handling network for the Hi-SIDE project: it is connected to each of the payload data-handling elements by a SpaceFibre link. The SpaceFibre network is used to transfer data at high data-rates between instruments, mass-memory, data compressor, data processor and downlink transmitters. It is also used to provide the control network used by the control computer to control both the network and the equipment attached to the network.

V. Hi-SIDE Demonstration

A block diagram of the Hi-SIDE demonstration system is shown in Figure 1. The various elements of the on-board data chain are shown on the left and right sides of the diagram interconnected via SpaceFibre links (red lines) to the routing switch in the middle of the diagram. Each element contains a SpaceFibre interface which connects it to the SpaceFibre network. The interfaces are either quad-lane or dual-lane interfaces, as shown by the number of the lanes in the link to the SpaceFibre routing switch. The interfaces have two or more virtual channels which are mapped by the routing switch to virtual networks. The virtual networks are colour-coded and a key to the type of traffic they handle is shown on the top, right-hand side of the diagram. The configured virtual networks are also illustrated inside the SpaceFibre routing switch (X = virtual network switch).

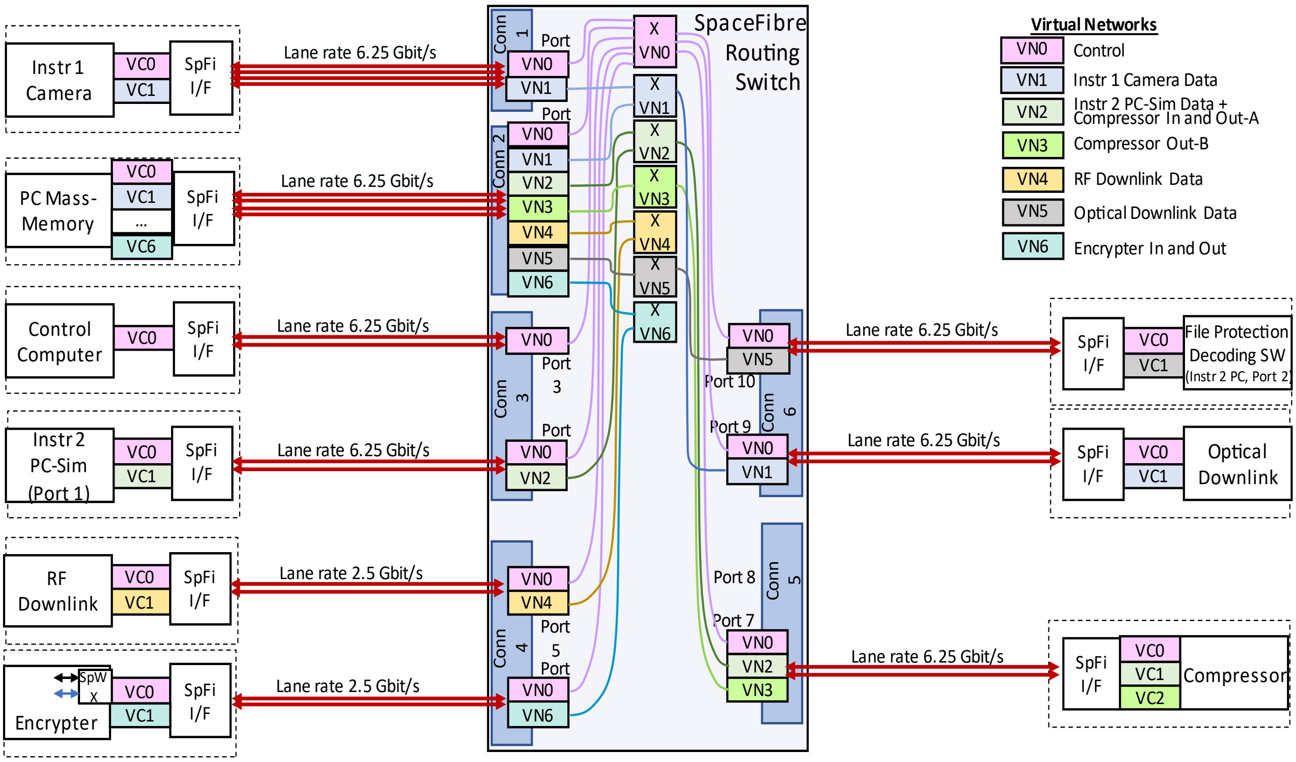

Figure 1: Hi-SIDE Demonstration System Block Diagram

VI. STAR-TIGER ROUTING SWITCH

The STAR-Tiger SpaceFibre routing switch [9] is shown in Figure 2 and comprises three circuit boards:

- An FPGA board containing an industrial grade Xilinx KU060 FPGA in which the SpaceFibre routing switch is implemented. The PCB footprint accommodates either the commercial/industrial part or the radiation tolerant part. The FPGA is surrounded by six Elara connectors which carry the electrical SpaceFibre signals. Each connector provides four lanes.
- A power supply board which provides nominal and redundant power input selection and delivers the five main power rails to the FPGA. Texas Instruments radiation tolerant power supply components are used. Other power rails are supplied by regulators on the other two boards.
- A configuration and scrubbing board. Configuration is from EEPROM or via a SpaceWire interface.

The main characteristics of the STAR-Tiger routing switch are listed below:

- 10 SpaceFibre ports:
  - Two quad-lane ports.
  - Eight dual-lane ports.
  - Lane speed up to 6.25 Gbit/s.
  - Port user data-rate up to 9.6 Gbit/s for a dual-lane port and 19.2 Gbit/s for a quad-lane port.
- 2 SpaceWire interfaces for programming the STAR-Tiger FPGA.
- Electronic components which are radiation-tolerant EM flight parts or industrial/commercial equivalents of flight parts.
- Spaceflight TRL5/6 level design.
- Power consumption of 14.2W, typical at 20 °C, with all links running and lanes speeds of 6.25 Gbit/s.
- Conduction cooled, with an operating temperature range: -25 to +55 °C.
- Size of 108 x 108 x 68 mm (excluding mounting brackets).

Figure 2: STAR-Tiger SpaceFibre Routing Switch

VII. HI-SIDE RESULTS

A photograph of the integrated demonstration system is shown in Figure 3.

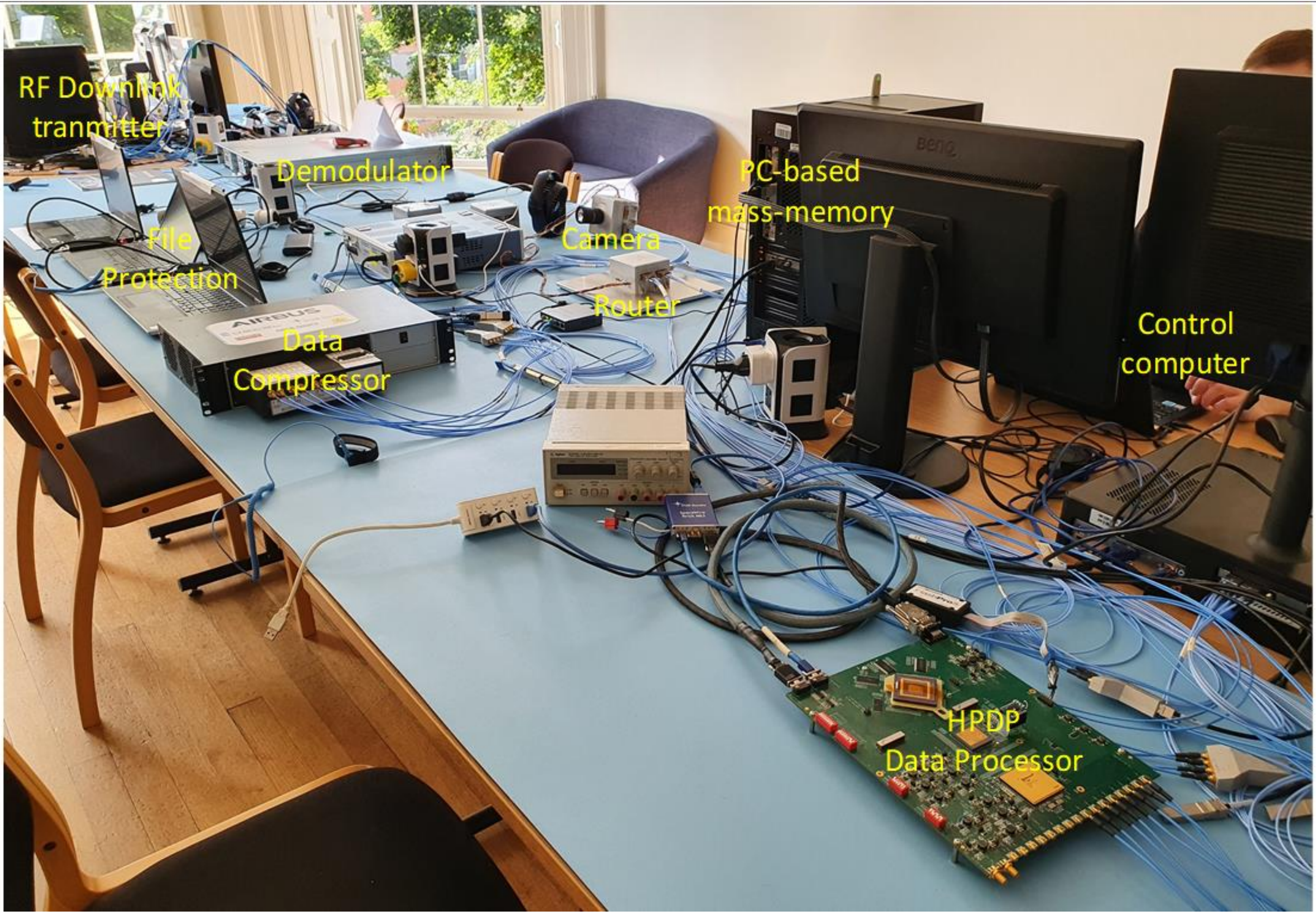

Figure 3: Photograph of the Integrated Hi-SIDE Demonstration System

The control computer was able to monitor and display the data rates of the traffic flowing through each virtual network during the demonstration. Figure 4 shows an example of traffic going to the mass-memory for storage. The chart shows data rates plotted over time for the VCs going into the Mass-Memory used to store data. In this diagram, the following data flows are shown:

- VC 1 (blue line): SpaceFibre Camera sending 8 GB of images to the Mass-Memory for storage.
- VC 2 (green line): Instrument 2 sending 16 GB of data to the Mass-Memory for storage and Data Compressor sending one half of the compressed data to the Mass-Memory for storage.
- VC 3 (purple line): Data Compressor sending the other half of the compressed data to the Mass-Memory for storage.

When these operations overlap, the total data rate of traffic being stored simultaneously in the Mass-Memory is around 14 Gbit/s (the SpaceFibre Camera is approximately 4.5 Gbit/s, Instrument 2 is approximately 9 Gbit/s and the Data Compressor is approximately 0.5 Gbit/s for each of the two compressed streams).

Further information on the Hi-SIDE demonstration system is available in [3].

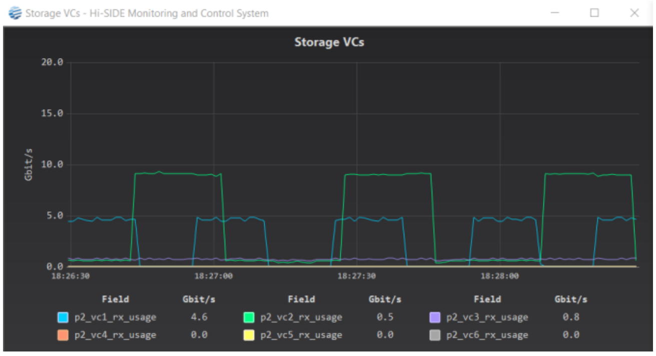

Figure 4: Example of Monitored Network Traffic to the Mass-Memory

VIII. SpaceFlight Processing Racks

As well as being used in distributed payload data-handling architectures, SpaceFibre is being used as a backplane interconnect in several standards for data-processing or payload data-handling units. A summary of these standards is provided in the following sections.

A. *VITA 78: SpaceVPX*

SpaceVPX [10] is the first standard for a payload data-handling and processing rack that uses SpaceFibre. SpaceVPX boards are either single or double Eurocard size. The most recent 2022 revision of SpaceVPX uses SpaceFibre as both a control and data-plane technology. Traditionally, SpaceVPX separates the various classes of traffic into four types: management, control, data and expansion. The management-plane is a low-level (I2C) interface for reading the type of module, monitoring temperature, voltages, etc., and for turning on power and resetting a module. The control-plane is normally a SpaceWire interface which is used to control the operation of the module. The data-plane is the primary interconnect for transferring data at high data-rates. The expansion-plane is for talking to an adjacent board so that a pair of boards can operate together in a similar way to a main board and mezzanine board, but with communication over the backplane.

The VCs of SpaceFibre separate different classes of traffic and provide resilience without the need for separate physical interconnect. This enables SpaceFibre to be used as both a control and data-plane. A dual-lane SpaceFibre link fits in a single SpaceWire control-plane slot. VC0 can then be used as the virtual control plane with a bandwidth allocation of, for example, 100 Mbit/s and set to high-priority. The other VCs can then be allocated to data transfers with a combined bandwidth allocation of 100 Mbit/s less than the full link bandwidth. With lane rates of 6.25 Gbit/s, the overall link bandwidth available for data is then around 9.5 Gbit/s (user data rate). A SpaceFibre routing switch on the SpaceVPX system controller module will then provide full interconnect between all modules in the rack at high data-rate.

B. *VITA 90: VNX+*

VNX+ [11] is a new VITA standard development based on the VNX standard which supports high data-rate interconnect. VNX is widely used in rugged terrestrial applications. VNX+ is being designed to support both terrestrial and space applications. SpaceFibre is one of the control and data-plane alternatives included in VNX+. VNX+ has a very small form factor and is ideal for CubeSat applications using COTS components.

C. *ESA ADHA*

The ESA Advanced Data-Handling Architecture (ADHA) [12] is a draft specification for a payload data-handling unit comprising several single or double Eurocard boards. It was originally based on the cPCI-Serial-Space standard, with substantial improvements being made. The ADHA specification is being developed by a closed group comprising ESA and the large European spacecraft prime manufacturers. There are three principal communication protocols that run over the backplane: CAN Bus, SpaceWire and SpaceFibre. The architecture is similar to SpaceVPX with a dual-star architecture between dual system controllers and up to eight "peripheral" slots (payload slots in SpaceVPX). In addition, there are two "extended peripheral" slots which are also connected via a dual-star network to all eight peripheral modules. The backplane connectors are Amphenol AirMax VS press-fit connectors, which are being qualified for space applications.

IX. Conclusions

SpaceFibre provides a high-performance, high-reliability and high-availability data-link and network technology for demanding applications. It is at TRL 9 - already in operation in space. SpaceFibre can be used as both a distributed network interconnect, as an interconnect between processing or data-handling boards inside a unit, and as an efficient interconnect between processors for high-performance, multi-processor data processing applications.

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