SpaceFibre Onboard Interconnect: from Standard, through Demonstration, to Space Flight

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Abstract— **SpaceFibre has been developed to provide a high data-rate, high-reliability, high-availability interconnect for spacecraft onboard applications [1]. Other drivers include a small footprint, simplicity of implementation, quality of service, and backwards compatibility with SpaceWire at the packet level. SpaceWire, developed in 2003, is now used as a moderate data-rate payload data-handling network on hundreds of space missions [2][3]. This paper describes the development of SpaceFibre from drafting of the standard, through development, testing and evaluation of key elements of the technology, to complete system-level demonstration, and finally to its first operational use in space.**

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1. INTRODUCTION

SpaceFibre [1] is a data link and network technology developed specifically for spacecraft on-board data-handling. It runs over electrical or fibre-optic physical layers. It uses latent multi-gigabit transceiver (MGT) technology available in current chips (FPGAs and ASICs) to provide data rates of tens and, in the near future, hundreds of Gbit/s. It automatically recovers rapidly from transient errors without loss of data, which has the welcome side-effect of improving the radiation tolerance of the multi-gigabit transceivers. It uses multiple lanes to achieve high data-rates, but also provides graceful-degradation and hot and cold redundancy for those lanes, in the case of a lane failure. Virtual channels with priority, bandwidth reservation and scheduling are used to form virtual networks which isolate different flows of data from one another. SpaceFibre also provides a low-latency broadcast message capability which can be used to distribute system time, to trigger or indicate the occurrence of events, to give notification of errors, etc.

Because of these important characteristics, SpaceFibre is now flying in several spacecraft and being designed into over 60 more.

2. SPACEFIBRE CAPABILITIES

The key features of SpaceFibre are outlined below [4]:

- High-performance, with 3.125 Gbit/s single-lane performance (including overhead for 8B/10B encoding) in the Microsemi RTG4, giving 12.5 Gbit/s with four lanes, and 6.25 Gbit/s per lane in Xilinx XQRKU060 and Microchip PolarFire, giving 25 Gbit/s with four lanes. Link rates of 40 Gbit/s are already in operation, with link rates of 100 Gbit/s expected soon.
- Electrical and fibre-optic media with the electrical medium supporting cable lengths up to 5m, depending on data rate, and fibre optics supporting up to 100m.
- High-reliability and high-availability using error-handling technology which is able to recover automatically from transient errors in a few

microseconds without loss of information and which is able to continue operation, preserving transfer of critical and important information when a lane in a multi-lane link fails.

- Multi-lane capability providing increased bandwidth aggregated into an overall link bandwidth, rapid (few microseconds) graceful degradation in the event of a lane failure, hot and cold lane redundancy, and support for asymmetric traffic with unidirectional lanes.
- Quality of service using multiple virtual channels across a data link, each of which is provided with a priority level, a bandwidth allocation and a schedule.
- Virtual networks that provide multiple independent traffic flows on a single physical network, which, when mapped to a virtual channel, acquire the quality of service of that virtual channel.
- Deterministic data delivery of information using the scheduled quality of service, in conjunction with priority and bandwidth allocation.
- Low-latency broadcast messages which provide time-distribution, synchronization, event signalling, error reporting and network control capabilities.
- Small footprint which enables a complete SpaceFibre interface to be implemented in a radiation tolerant FPGA, for example, around 3% of an RTG4 FPGA for a typical instrument interface with two virtual channels.
- Backwards compatibility with SpaceWire at the network level, which allows simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.

3. SPACEFIBRE PROTOCOL STACK

In this section an overview of the SpaceFibre protocol stack is provided along with the services it provides. The SpaceFibre protocol stack is illustrated in Figure 1.

SpaceFibre provides three services to the user application:

A **packet transfer service** which is used to send and receive packets. SpaceFibre packets have the same form as SpaceWire packets making it simple to connect between SpaceWire and SpaceFibre networks.

A **broadcast message service** which is used to broadcast short messages over the SpaceFibre network. This can be used for broadcasting system time information, synchronization signals, equipment events, interrupts, and network management information, all with very low latency. It can also be used to carry SpaceWire time-codes over a SpaceFibre network.

A **management service** which is used for configuring, controlling and monitoring the status of a SpaceFibre interface, device or network.

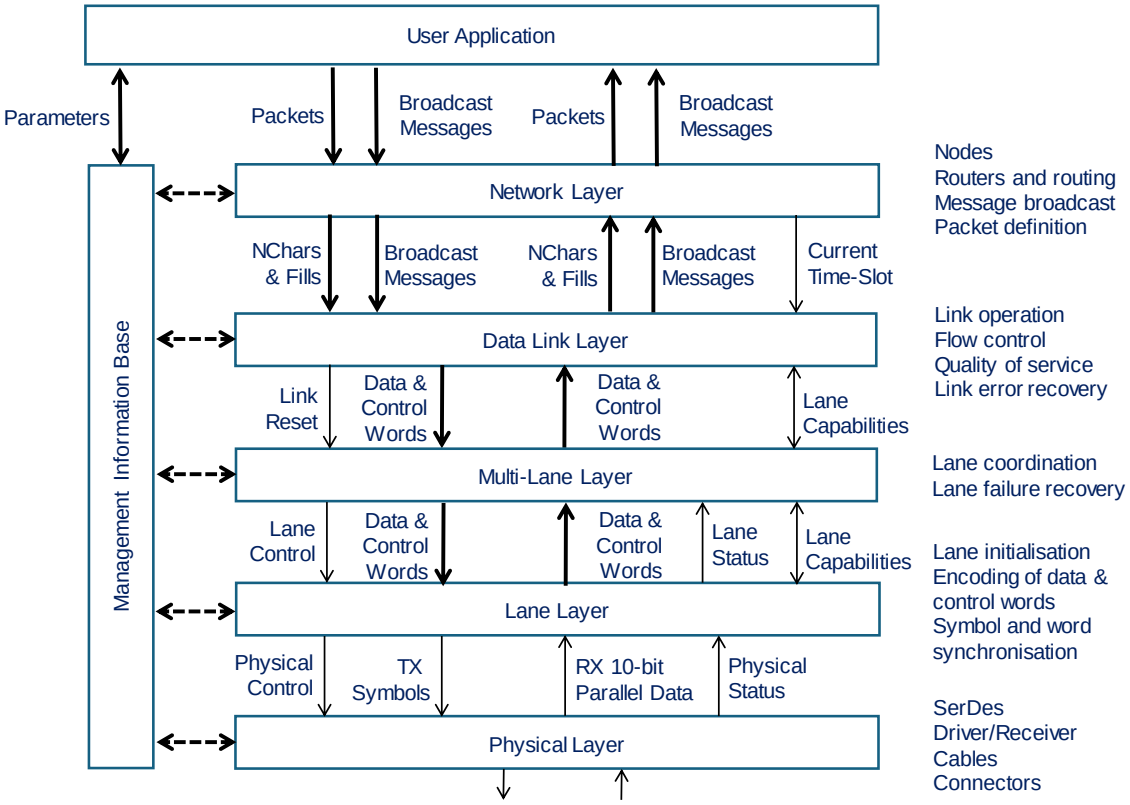

Figure 1. SpaceFibre Protocol Stack

The **Network layer** is responsible for transferring packets over a SpaceFibre link or network. The information to be sent is packaged in the same format as SpaceWire: <Destination Address><Cargo><EOP>. It uses the same routing concepts as SpaceWire including both path and logical addressing, and uses a special EOP marker to indicate the end of a packet. The Network layer is also responsible for broadcasting short messages across the SpaceFibre network and for receiving and checking those messages.

The **Data Link layer** provides quality of service, flow control and error handing for a SpaceFibre link. It sends packet information in frames of up to 64 data words (256 bytes) on each lane. The Data Link layer is responsible for the overall operation of the link, the quality of service and link error recovery. Virtual channels are used to provide separate packet streams and to support the various qualities of service: priority, bandwidth reservation and scheduling. Data packets from each virtual channel are segmented into frames which are interleaved over the SpaceFibre link according to available flow control and QoS information. In the event of an error occurring on the SpaceFibre link, the error is detected and recovered rapidly.

The **Multi-Lane layer** operates two or more SpaceFibre lanes in parallel to provide higher data throughput and redundancy with graceful degradation. In the event of one lane failing the remaining lanes will automatically share the load, resulting in continuous operation with reduced capacity. The Multi-Lane layer is responsible for lane coordination and lane failure recovery.

The **Lane layer** initializes each lane and performs error recovery when an error is detected. Data is encoded into symbols for transmission using 8B/10B encoding and these symbols are decoded in the receiver. 8B/10B codes are DC balanced, supporting AC coupling of SpaceFibre interfaces. The Lane layer is responsible for the individual lanes providing lane initialization and encoding of data and control words.

The **Physical layer** serializes the 8B/10B symbols and sends them over the physical medium. Both electrical cables and fibre-optic cables are supported by SpaceFibre. The Physical layer is responsible for the serialization and de-serialization (SerDes), electrical driver and receiver, connectors and cables. Flight connectors and cables for both electrical and fibre-optic media are specified.

The **Management Information Base** supports the configuration, control and monitoring of all the layers in the SpaceFibre protocol stack.

From the OSI perspective, the Multi-Lane layer and Lane layer are sub-layers of the Data Link layer. The Lane layer defines functionality which is specific to a single lane or to each of several lanes in a multi-lane link. The Multi-Lane layer defines functionality which is specific to a multi-lane link. The Data Link layer defines functionality which is common to single-lane and multi-lane links. The SpaceFibre ECSS standard provides a set of service interfaces for the Network, Data Link and Physical layers of the protocol stack, along with the service interface for the Management Information Base.

4. SPACEFIBRE DEVELOPMENT

The early research on SpaceFibre was carried out primarily by the University of Dundee and STAR-Dundee. The goals of SpaceFibre were to provide:

- a data link and network technology which was backwards compatible with SpaceWire at the packet level,
- a substantial increase in performance compared to SpaceWire (factor of 10 to 100 improvement),
- fault detection, isolation and recovery capabilities,
- quality of service,
- a small footprint, i.e. use as few FPGA/ASIC resources as possible,
- ability to operate over fibre optic or electrical media,
- broadcast message capability that could carry some user information in the message.

Early Research

The early research on SpaceFibre developed the Lane and Link layers including the quality of service (QoS) and fault detection isolation and recovery (FDIR) capabilities [5]. All through the development, efficiency of implementation was a critical driver. The QoS provides flow-control, bandwidth reservation, priority, and scheduling of data over multiple virtual channels. Data from the virtual channels is split into small frames and interleaved over the Physical layer to fulfil the required QoS settings of the virtual channels.

SpaceFibre IP cores were designed, tested in simulation, implemented in hardware, tested and the whole process iterated many times to achieve the required functionality, robustness, and small footprint needed for space applications. The Very High Speed Serial Interface (VHiSSI) European Commission Framework 7 project designed and evaluated technology suitable for implementation of SpaceFibre very high-speed serial interfaces for spaceflight applications [6][7].

The University of Dundee and STAR-Dundee designed, simulated, tested and evaluated various design alternatives for different aspects of SpaceFibre. FPGA-based implementations of SpaceFibre were run in real-time to hone the emerging technology.

Substantial effort went into the specification, testing and validation of SpaceFibre, by the University of Dundee, STAR-Dundee and other organizations across the world. Following successful interoperability testing of independent implementations, emphasis moved on to completing the

SpaceFibre specification and getting the technology ready for spaceflight. To this end STAR-Dundee developed a SpaceFibre Interface IP Core, which was validated and beta tested in several different applications.

SpaceFibre Interface on Microchip RTG4

The availability of the Microchip RTG4 FPGA provided radiation tolerant SerDes in a powerful, radiation tolerant FPGA. The RTG4 FPGA is fully reprogrammable with an integrated flash memory to store configuration information. It contains 151,824 logic elements, 209 blocks of dual-port SRAM, 210 three-port SRAM blocks, two high-speed DDR2/DDR3 memory controllers and 462 math blocks. Critically for SpaceFibre the RTG4 includes 24 high-speed (3.125 Gbit/s) serial interfaces integrated on-chip.

STAR-Dundee implemented a SpaceFibre interface on the RTG4 Development Board. The SpaceFibre interface operated at 2.5 Gbit/s initially and with a little more work it operated at 3.125 Gbit/s. The SpaceFibre single-lane interface took around 2 to 5% depending on the number of virtual channels supported, see Table 1 [8].

The use of the SpaceFibre interface IP core on the RTG4 provided a powerful platform for spacecraft on-board data-handling and instrument interfacing. Furthermore, the advanced QoS and FDIR capabilities of SpaceFibre made it suitable for a wider range of spacecraft on-board applications including integrated payload data-handling and attitude and orbit control networks and launcher applications where deterministic data delivery is required.

	RTG4			XQRKU060 [1]		
	LUT	DFF	RAM	LUT	DFF	RAM
1 VC	2.0%	1.5%	1.9%	0.5%	0.3%	0.4%
2 VC	2.4%	1.8%	2.9%	0.6%	0.4%	0.6%
4 VC	3.2%	2.6%	4.8%	0.9%	0.6%	0.9%

	RTPF500T [1]			XQRVC1902 [1]		
	LUT	DFF	RAM	LUT	DFF	RAM
1 VC	0.6%	0.4%	0.5%	0.2%	0.1%	0.4%
2 VC	0.7%	0.6%	0.8%	0.2%	0.2%	0.6%
4 VC	0.9%	0.8%	1.3%	0.3%	0.2%	1.0%

[1] TMR not included

Table 1. Utilization of STAR-Dundee's SpaceFibre Single-Lane Interface on Various Space Grade FPGAs

SpaceFibre Multi-Lane

The multi-lane capabilities of SpaceFibre have been designed to meet the following requirements [9]:

1. Support an arbitrary number of lanes, which allows redundancy and graceful degradation without any restriction on the number of lanes.
2. Re-synchronize both ends of a link when the number of lanes changes, without resetting any lane, so that recovery is as fast as possible.
3. Support hot redundancy.
4. Support dynamic unidirectional lanes to save power and mass for asymmetric user data flows.
5. Be robust against lane errors and misconfiguration.
6. Keep the number of lanes independent from the width of the end-user interface.

The SpaceFibre multi-lane interface was designed by first creating and evaluating the key concepts that could allow the requirements to be met (e.g. by defining generic protocol sequence diagrams). These concepts were then constrained to work with the more specific set of rules already specified in the SpaceFibre standard (e.g. adapting them to the control word definitions). The concepts were validated using a software simulator that could be easily modified. When issues were found, the concepts and set of rules were reworked. The simulation engine was refined to validate the proposed multi-lane specifications with high accuracy.

		RTG4			XQRKU060 [1]		
		LUT	DFF	RAM	LUT	DFF	RAM
2 Lanes	1 VC	4.5%	3.6%	3.8%	0.9%	0.7%	0.7%
	2 VC	5.0%	4.1%	5.7%	1.1%	0.8%	1.1%
	4 VC	6.0%	5.1%	9.6%	1.3%	1.0%	1.9%
4 Lanes	1 VC	8.6%	6.4%	7.7%	1.7%	1.2%	1.1%
	2 VC	9.2%	7.1%	11.5%	1.9%	1.3%	1.7%
	4 VC	10.3%	8.5%	19.1%	2.1%	1.6%	2.8%
8 Lanes	1 VC	18.8%	11.9%	15.3%	3.5%	2.1%	1.9%
	2 VC	19.5%	13.0%	23.0%	3.7%	2.3%	2.8%
	4 VC	21.1%	15.1%	38.3%	4.2%	2.8%	4.6%

		RTPF500T [1]			XQRVC1902 [1]		
		LUT	DFF	RAM	LUT	DFF	RAM
2 Lanes	1 VC	1.1%	0.9%	0.8%	0.3%	0.3%	0.8%
	2 VC	1.3%	1.0%	1.2%	0.4%	0.3%	1.2%
	4 VC	1.6%	1.4%	2.0%	0.5%	0.4%	2.1%
4 Lanes	1 VC	2.1%	1.5%	1.3%	0.6%	0.4%	1.2%
	2 VC	2.3%	1.7%	2.0%	0.6%	0.5%	1.9%
	4 VC	2.6%	2.1%	3.3%	0.7%	0.6%	3.1%
8 Lanes	1 VC	4.7%	2.7%	2.4%	1.2%	0.8%	2.1%
	2 VC	5.0%	3.1%	3.6%	1.3%	0.9%	3.1%
	4 VC	5.4%	3.7%	5.9%	1.4%	1.0%	5.2%

[1] TMR not included

Table 2. Utilization of STAR-Dundee's SpaceFibre Multi-Lane Interface on Various Space Grade FPGAs

After the new specifications for the multi-lane capabilities were successfully simulated in software, a hardware prototype was built using first commercial off-the-shelf (COTS) and then space-qualified FPGAs. The resulting SpaceFibre multi-lane interface IP Core was then optimised and improved, reducing the footprint, enhancing performance, and resolving issues found through extensive testing.

The goals of the SpaceFibre Multi-Lane layer were achieved resulting in a highly capable and resource efficient multi-lane interface IP core for SpaceFibre. The resource utilization of STAR-Dundee's SpaceFibre multi-lane interface IP core implemented on various space grade FPGAs is presented in Table 2.

SUNRISE: The First SpaceFibre Router

The first SpaceFibre router was designed, implemented and tested in the SUNRISE project funded by the UK Space Agency and STAR-Dundee [10]. The architecture of this router is shown in Figure 2.

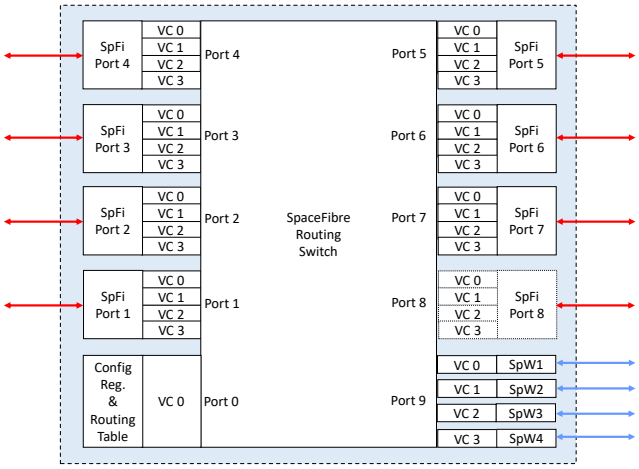

Figure 2. SUNRISE SpaceFibre Router Architecture

The SUNRISE router has eight SpaceFibre ports, numbered 1 to 8, each with four virtual channels. There is a configuration port (port 0) which is used for device configuration, and which can be accessed using virtual channel 0 of any of the other ports. Another port (port 9) provides an interface to four SpaceWire ports using four virtual channels, one for each SpaceWire port. SpaceWire and SpaceFibre packets are switched by the routing switch in the same way, using the leading data character of a packet to determine the output port that the packet is to be switched to. Both path and logical addressing can be used with the SUNRISE router.

The SUNRISE router was implemented initially in a Xilinx Spartan 6 FPGA on a STAR-Dundee PXI board and subsequently on a STAR-Dundee PXIe-RTG4 board which uses the radiation tolerant Microsemi RTG4 FPGA. Power is taken from the backplane and the eight SpaceFibre and four SpaceWire ports are available on the 40mm wide front panel. The prototype SUNRISE router is shown in Figure 3.

Various experimental modes of operation were included in the SUNRISE router design to explore different routing concepts. This was used to help validate the characteristics of the SpaceFibre Network layer as the standard document was being written.

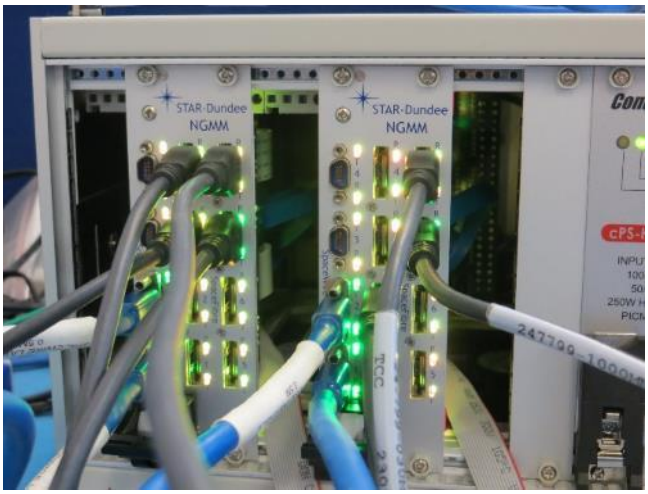

Figure 3. SUNRISE SpaceFibre Routers Under Test

SpaceFibre Camera

The SpaceFibre camera is a high-resolution, high frame-rate camera which demonstrates the suitability of SpaceFibre as an instrument interface [11]. It incorporates the Microchip RTG4 FPGA which, as well as providing the image sensor interface, control logic and SpaceFibre interfaces, has plenty of room left for data compression or other image processing applications to be integrated in the camera.

A 2k x 2k pixel image sensor is configured and controlled by the RTG4 FPGA. The image sensor sends image data to the FPGA via 16 LVDS differential pairs running at up to 480 Mbit/s per pair. The FPGA includes four SpaceFibre lanes which can operate as two 2-lane links or one 4-lane link. When operating with two 2-lane links, one is active and the other is redundant. The FPGA transfers the image data out of the camera over the active SpaceFibre link.

Camera configuration, control and housekeeping requests are received over Virtual Channel 0 (VC0) of the active SpaceFibre link. The FPGA interprets these commands and transfers information to and from the image sensor accordingly, using the control interface of the image sensor. There is no processor inside the camera. Configuration, control and housekeeping are carried out using the Remote Memory Access Protocol (RMAP) running over VC0.

The SpaceFibre camera electronics is implemented on a single flexi-rigid PCB as illustrated in Figure 4. The blue areas represent the rigid part of the PCB and the green the flexible part. The power supply circuitry is on one board,

along with the SpaceWire connectors, and power supply/configuration connectors. The RTG4 is on the middle board, together with the DDR memory and the four SpaceFibre connectors, to minimise the PCB track lengths from the FPGA. The image sensor is on the third board, along with the power supplies for the image sensor. The LVDS lines from the image sensor run through the flexi part of the PCB to the FPGA. The complete camera is shown in Figure 5.

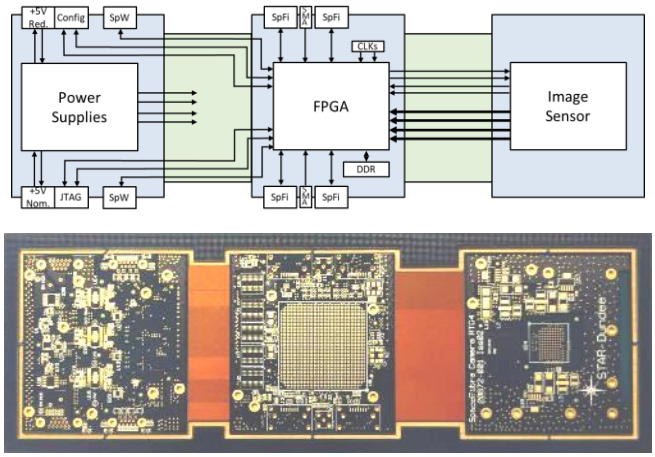

Figure 4. SpaceFibre Camera PCB

Figure 5. SpaceFibre Camera

STAR-Tiger Multi-lane Router

A SpaceFibre network is formed by a SpaceFibre routing switch, the SpaceFibre interfaces in each payload data-handling element (instruments, mass-memory unit, data processors and downlink transmitter), and the SpaceFibre cable assemblies that connect them all together. The STAR-Tiger SpaceFibre multi-lane routing switch was developed by STAR-Dundee to demonstrate SpaceFibre networks running with user data rates of up to 19.2 Gbits/s per link [12].

A photograph of the STAR-Tiger SpaceFibre routing switch is shown in Figure 6.

Figure 6: STAR-Tiger SpaceFibre Routing Switch

The STAR-Tiger SpaceFibre multi-lane routing switch has the following key features:

- 10 SpaceFibre ports
  - Two quad-lane ports
  - Eight dual-lane ports
  - Lane speed up to 6.25 Gbit/s
  - Port user data-rate up to 9.6 Gbit/s dual-lane port and 19.2 Gbit/s quad-lane port
- Bisection bandwidth is 115 Gbit/s (user data-rate)
- Spaceflight TRL-6 level design
- Electronic components are radiation tolerant EM flight parts or industrial/commercial equivalents of flight parts
- Power consumption is 14.2W typical at 20 °C, with all links running at lane speeds of 6.25 Gbit/s
- Conduction cooled
- Operating temperature range: -25 to +55 °C
- 108 x 108 x 68 mm (excluding mounting brackets)

The STAR-Tiger boards were subject to extensive testing during development and integration. Once STAR-Tiger was operational, verification tests were carried out to ensure that the unit performed as required. The test setup used for many of the functional tests is shown in Figure 7. The STAR-Tiger routing switch was tested using the STAR-Dundee STAR-Ultra PCIe SpaceFibre interface board [13].

At this point STAR-Dundee had a complete set of validated SpaceFibre IP cores ready for, and being designed into, spaceflight applications.

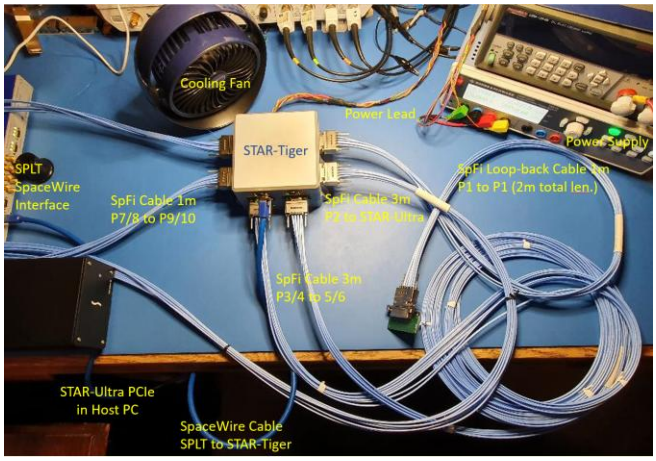

Figure 7. STAR-Tiger Test Setup

5. SPACEFIBRE STANDARDS

The SpaceFibre standard was written by Steve Parkes at the University of Dundee (now CTO of STAR-Dundee) with inputs from international engineers via the SpaceWire Working Group, which was open to spacecraft engineers from across the world. The University of Dundee and STAR-Dundee developed and proved the technology before it was incorporated in the SpaceFibre standard. Funding for this work was provided by STAR-Dundee, European Union, UK Space Agency and ESA. As each major draft of the standard was written it, and the technology behind it, was presented to the SpaceWire Working Group for comment.

SpaceFibre ECSS Standard

By September 2015, the SpaceFibre standard was already in a fairly mature state (at Draft H1 and already written in ECSS format). An ECSS working group was then set up by ESA with Martin Suess (ESA) as Convenor and Steve Parkes as Editor to complete the work on the standard. The ECSS-E-ST-50-11C "SpaceFibre – Very High-Speed Serial Link", standard was published in May 2019. The ECSS working group was formed from ESA member states only, however, the SpaceWire Working Group members were kept informed of progress and invited to make comments on each emerging draft of the standard.

The ECSS-E-ST-50-11C SpaceFibre standard is an open standard available with no charge from the ECSS website [1].

Because of its high-performance, high-availability and small footprint SpaceFibre has been adopted not only as a unit-to-unit interconnect technology, but as a backplane interconnect within a unit. It has been incorporated in the SpaceVPX and ADHA standards, and is being incorporated in SpaceVNX+. These standards will now be described.

SpaceFibre in SpaceVPX

SpaceVPX, VITA78.0-2022 [14], was the first standard for a payload data-handling and processing rack that incorporated SpaceFibre. SpaceVPX boards are either single or double Eurocard size. The most recent 2022 revision of SpaceVPX uses SpaceFibre as both a control- and data-plane technology. Traditionally, SpaceVPX separates the various classes of traffic into four types: management, control, data and expansion. The management-plane is a low-level (I2C) interface for reading the type of module, monitoring temperature, voltages, etc., and for turning on power and resetting a module. The control-plane is normally a SpaceWire interface which is used to control the operation of the module. The data-plane is the primary interconnect for transferring data at high data-rates. The expansion-plane is for talking to an adjacent board so that a pair of boards can operate together in a similar way to a main board and mezzanine board, but with communication over the backplane. The control-plane is normally a star or dual-star network with routing switches on the system controller boards or on a separate network switch board.

SpaceFibre in ESA ADHA Specification

The ESA Advanced Data-Handling Architecture (ADHA) [15] is a draft specification for a payload data-handling unit comprising several single or double-extended Eurocard boards. It was originally based on the cPCI Serial Space standard, with substantial improvements being made. The ADHA specification is being developed by a closed group comprising ESA and the large European spacecraft prime manufacturers. There are three principal communication protocols that run over the backplane: CAN Bus, SpaceWire and SpaceFibre. The architecture is similar to SpaceVPX with a dual-star architecture between dual system controllers and up to eight "peripheral" slots (payload slots in SpaceVPX). In addition, there are two "extended peripheral" slots which are also connected via a dual-star network to all eight peripheral modules.

SpaceFibre in SpaceVNX+

VNX+, VITA90.x [16], is an emerging VITA standard for small form-factor systems which is based on the earlier VNX standard. VNX is widely used in aerospace and military terrestrial applications.

SpaceVNX+ is a version of VNX+ specifically being designed for space applications. It can support single-string, dual-redundant and 1-of-M redundant architectures to suit various application reliability levels. SpaceFibre is one of the control and data-plane interconnect protocols included in SpaceVNX+. SpaceVNX+ has a very small form factor and offers high-performance and relatively low power consumption. Further information is available for VITA members on their website [16].

SpaceVNX+ is currently in its definition and prototyping stage with drafting of the formal standard expected to start in 2025.

6. SYSTEM-LEVEL DEMONSTRATION

The Hi-SIDE project developed critical technologies for handling and transferring data from instruments to processing

and storage elements on-board a spacecraft, and to the downlink transmitters that send data to ground [17]. The Hi-SIDE payload data-handling architecture is fully distributed with several instruments, payload data-handling units and downlink transmitters connected together using a SpaceFibre network. A demonstration system, representative of an Earth observation mission with demanding on-board data rates, was implemented. A photograph of the Hi-SIDE demonstration system is shown in Figure 8.

The Hi-SIDE demonstration system contained the following elements of the data chain.

- Camera providing real-time images at a data rate of around 4.6 Gbit/s (STAR-Dundee).
- Instrument simulator providing hyperspectral data (or other forms of data) at a data rate of around 9 Gbit/s (STAR-Dundee).
- Mass-memory simulator [18] implemented in a PC with SpaceFibre interface. Data rates into the mass-memory of up to 14 Gbit/s are possible (STAR-Dundee).

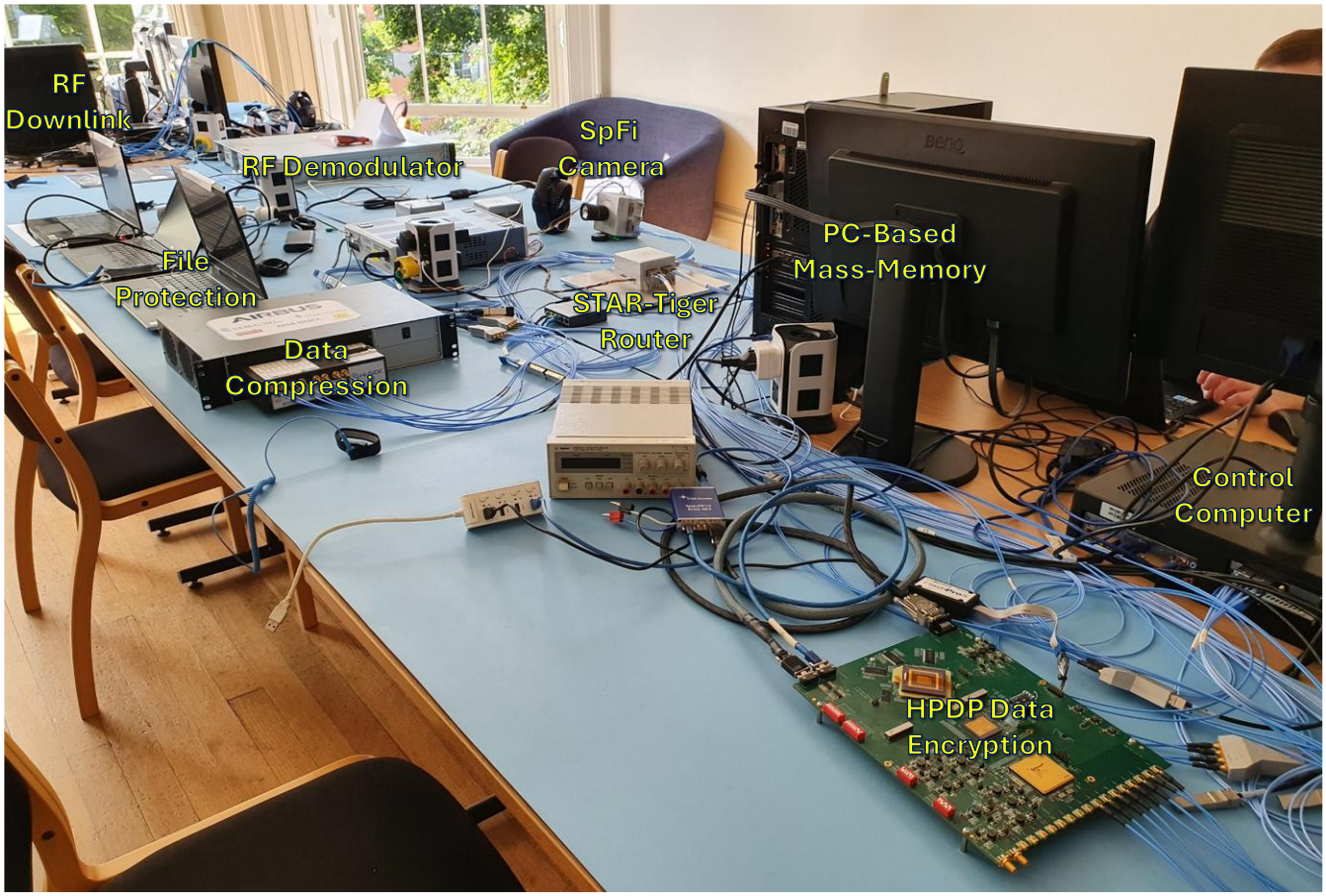

Figure 8. Photograph of the Integrated Hi-SIDE Demonstration System

- Control Computer (PC-based) [18] which is used to configure, control and monitor the SpaceFibre network and equipment connected to the network (STAR-Dundee).
- Data compressor [19] which performs CCSDS 123.0-B-2 Low-Complexity Lossless and Near-Lossless Multispectral and Hyperspectral Image Compression at data rates of around 7.5 Gbit/s (Airbus and NKUA).
- Low power consumption High-Performance Data Processor (HPDP) [20] which was programmed to perform data encryption (ISD).
- Radio Frequency (RF) downlink [21] (TESAT designing the modulator, ERZIA developing an RF power amplifier and Kongsberg developing a demodulator).
- Optical downlink simulator - an image viewer which replaced the optical downlink [22] in the final demonstration. The 10 Gbit/s optical downlink was demonstrated separately due to component availability issues (DLR).
- File Protection Scheme (FPS) [23] for protecting data from gaps in the optical data stream caused by atmospheric effects (DLR).

- SpaceFibre Multi-Lane Routing Switch [12] interconnecting the units together in a simple star network (STAR-Dundee).

The STAR-Tiger SpaceFibre routing switch is the primary element of the Hi-SIDE payload data-handling network. It is connected to each of the payload data-handling elements by a SpaceFibre link. The SpaceFibre network is used to transfer data at high data-rates between instruments, mass-memory, data compressor, data processor and downlink transmitters. It is also used to provide the control network used by the control computer to control both the network and the equipment attached to the network.

The camera, data compressor, HPDP, RF downlink and optical downlink all incorporated the STAR-Dundee Multi-Lane SpaceFibre interface IP core so they could connect to the SpaceFibre network. Various types of FPGA were used on the different units. The instrument simulator, mass-memory simulator and control computer used the STAR-Dundee STAR-Ultra PCIe board [13] which provides a high-speed interface between SpaceFibre and a host PC.

The Hi-SIDE project was presented with the Innovation in Space Award from the European Space Forum in 2022 [24].

7. SpaceFibre in Space

SpaceFibre is now flying in at least six operational spacecraft and is currently being designed into more than sixty other spacecraft. The first flights of SpaceFibre were on experimental CubeSats, where SpaceFibre links were tested in the space environment. Shortly afterwards SpaceFibre was flying in its first operational missions.

Pléiades NEO 3 and 4

One of the first, if not the first, operational mission that SpaceFibre flew on was Pléiades NEO 3, which was developed by Airbus and launched in April 2021. It was followed shortly afterwards by Pléiades NEO 4, which was launched in August 2021. These two identical spacecraft provide very high resolution (30 cm) optical imagery and are phased 180° from each other in orbit, to provide rapid revisit time [25].

The payload data-handling system on-board these two spacecraft, took advantage of the capabilities and radiation tolerance of the Microchip RTG4 FPGA. A simplified block diagram is shown in Figure 9 [26]. The device provides data compression, data recording and ciphering functions. To handle the high data-rate from the image sensors, a SpaceFibre network was used to connect several of the FPGAs together, running in parallel. The demanding design required 79% of the FPGA, so the small footprint and high performance of the SpaceFibre interface was essential.

Pléiades NEO 3 and 4 are currently operational, having been designed for a 10-year life. Unfortunately the Vega C launcher carrying Pléiades NEO 5 and 6 into orbit failed, resulting in the loss of both satellites.

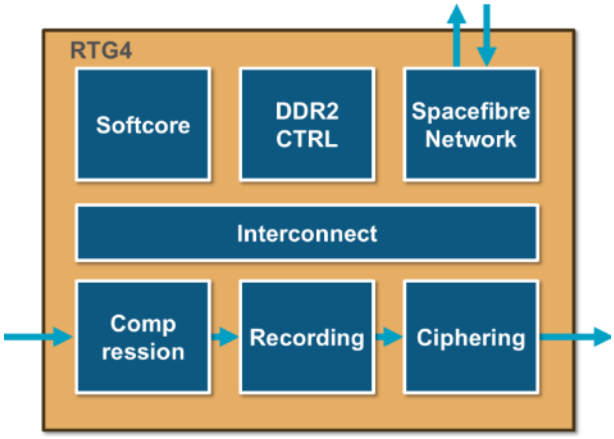

Figure 9. Pléiades NEO 3 Simplified FPGA Architecture

Other Space Applications

SpaceFibre is being designed into many more missions, in both the USA and Europe, the details of which are under NDA. These missions use various combinations of STAR-Dundee's SpaceFibre single-lane and multi-lane interfaces and routing switch IP cores.

Spectrometer for HyMS IOD Mission

The WBS-VIII is a wideband spectrometer (WBS) which is being developed to fly on the Hyperspectral Microwave Sounder (HyMS) In-Orbit Demonstrator (IOD) being developed by Spire [27]. WBS-VIII is an 8-channel FFT-based spectrum analyzer being designed by STAR-Dundee, which processes a total bandwidth of around 16 GHz to better than 10 MHz resolution [28]. The acquired spectra are accumulated within the WBS-VIII over a programmable integration time, substantially reducing the data rate to a modest data rate. The resulting spectra are sent to an Instrument Control Unit (ICU) over a SpaceFibre link. The SpaceFibre interface is also used to configure, control and monitor the WBS-VIII. The ICU sends trigger broadcast messages over SpaceFibre to the WBS-VIII to control the timing of data acquisition which is synchronized to the position of the instrument antenna. A photograph of the WBS-VIII flight model, ready for delivery is shown in Figure 10.

Figure 10. WBS-VIII Flight Model

SpaceFibre is normally used to provide high data-rate interconnect. The data-rate of the WBS-VIII is within the capabilities of a SpaceWire interface, so why was SpaceFibre used? There are several reasons which are listed below:

- Availability of Serializers/De-serializers (SerDes) - otherwise known as Multi-Gigabit Transceivers (MGT). Many FPGAs now include MGTs making the inclusion of SpaceFibre in a device possible.

- Low Power of the MGTs - MGTs embedded in recent FPGAs have very low power consumption.

- Low Mass, Flexible Cable - The mass of the SpaceFibre electrical cable is much less than that of a SpaceWire cable (around half the mass) and the SpaceFibre cable is much more flexible. This simplifies cable routing and makes routing of cables through tight spaces possible.

- Broadcast Messages - Broadcast messages are short, low-latency messages that are broadcast across a SpaceFibre network. They can be used, amongst other things, in place of normal trigger in/out signals, saving connectors and mass, and improving reliability. In the WBS-VIII broadcast messages are used for triggering, providing status information, and for early indication of fault conditions.

SpaceFibre has been used as the interface to an instrument processor unit, the WBS-VIII, which does not need the high data-rates that SpaceFibre provides. The many capabilities of SpaceFibre enable it to provide services that would not normally be thought of, which not only reduce hardware complexity, but also simplify the software in the ICU controlling the WBS-VIII.

8. FIBRE OPTIC MEDIA

It remains to consider fibre optic media for SpaceFibre. The SpaceFibre standard specifies 850 nm wavelength optical signals running over multi-mode, 50/125 µm graded-index fibre. The SpaceFibre Type-B fibre optic medium includes the use of the MT-Ferrule contacts.

Fibre optic media offers several advantages over electrical interconnect:

- High speed – radiation tolerant fibre optic transceivers are available, or under development, which support quad-lane links operating at 10 Gbit/s per lane, supporting an aggregate data rate of 40 Gbit/s in each direction [29][30][31]. A 28 Gbit/s quad lane transceiver is also available, giving an aggregate data rate of over 100 Gbit/s [29]. Ruggedized fibre optic cables are available from several organizations.

- Long distance – fibre optic media has very low loss, so that distances of up to 100 m are possible with SpaceFibre running over fibre optic cable. The SpaceFibre protocol sets a maximum distance of 100 m, which is more than most spacecraft require, so that the link-level error recovery is fast and the error recovery buffers are small.

- Galvanic isolation – complete galvanic isolation between the two ends of a link is possible, which might be useful for some space applications.

- Reduced Electro-Magnetic Interference (EMI) – the optical interconnect removes any possible ground loops associated with common-mode signal return currents, improving EM emissions.

- Low cable mass – fibre optic cable is substantially lighter than electrical cable. To achieve longer distances using copper cable a larger, lower-loss conductor is required so the mass increase with distance is greater than might be expected. Hence, the further the distance the greater the mass advantage of fibre optics.

- Tight bend radius – fibre optic cable has a tight bend radius so that it is easy to integrate in a harness. Multi-lane fibre optic ribbons have a tight bend radius in one dimension.

- Easy to use connectors – the SpaceFibre Type-B fibre optic medium includes the use of MT-Ferrule contacts. MT-ferrules that can take 8, 12 or 24 fibres are now used widely. The MT-ferrule can be inserted in a wide range of connector shells including shells for backplane interconnect in the SpaceVPX and SpaceVNX+ standards. Bulkhead connections are trivial using MT-ferrules.

These substantial advantages come at the cost of:

- Increased power consumption – the power consumption of a 10 Gbit/s per lane fibre optic transceiver is around 100 to 115 mW per lane, which is less than 500 mW for a quad-lane link. It is around 160 to 330 mW per lane at 28 Gbit/s lanes.

- Increased PCB area – additional PCB area is required for the fibre optic transceiver. The footprint of space grade quad-lane fibre optic transceivers vary from approximately 1 to 3.3 cm^2. Some devices are significantly larger.

When the required data rate is greater than around 6.25 Gbit/s per lane or the distance to be covered is greater than several meters, fibre optics becomes a very attractive medium for SpaceFibre.

9. CONCLUSIONS

The principal results of this work are:

- A standard published by the European Cooperation for Space Standardization.

- A system-level demonstration interconnecting instruments, mass-memory, data-compressor, data-encryptor, radio frequency downlink and optical downlink through a SpaceFibre routing switch with a bisection bandwidth of over 100 Gbit/s.

- SpaceFibre flying in and being designed into important space missions.

SpaceFibre provides a high-performance, high-reliability and high-availability data-link and network technology for demanding applications. It is at TRL 9 - already in operation in space. SpaceFibre can be used as both a distributed network interconnect, as an interconnect between processing or data-handling boards inside a unit, and as an efficient interconnect between processors for high-performance, multi-processor data processing applications.

SpaceFibre is now flying in at least six operational spacecraft and around 60 more are under development. SpaceFibre is a data and control plane technology in the VITA 78.0-2022 SpaceVPX standard, a high-speed interconnect in the ESA Advanced Payload Data Handling specification, and is also being used in the emerging SpaceVNX+ standard.

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BIOGRAPHY

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Albert Ferrer-Florit *has a PhD in high-speed interconnection networks for space applications awarded by the University of Dundee. His PhD research was funded by ESA's Networking/ Partnering Initiative after he worked in the on-board data processing group (TEC-EDP) in ESTEC. He is specialised in SpaceWire and SpaceFibre networks, being one of the key developers of the SpaceFibre standard. He started his career at CERN in the Summer Student Programme, worked for STAR-Dundee and currently works for STAR-Dundee as a Network and Chip Designer.*

Alberto Gonzalez Villafranca *holds a doctorate in data compression for space applications and has been connected to the space field throughout his entire professional career. He began by collaborating with the Gaia mission and subsequently worked on the hardware implementation of a deterministic variant of the SpaceWire protocol at the European Space Agency. Since then, Alberto has been deeply involved in the definition and implementation of SpaceFibre for more than 10 years, first with STAR-Dundee Ltd and later with its subsidiary, STAR-Barcelona, as a Chip Designer.*

Dave Gibson *received a BSc. in Applied Computing and a PhD from the University of Dundee, where he focused on SpaceWire-D, a deterministic protocol running on top of existing SpaceWire networks and technology. Since 2015, he has been a software engineer at STAR-Dundee working on a variety of SpaceWire and SpaceFibre applications including Remote Direct Memory Access over SpaceFibre, SpaceWire and SpaceFibre software for embedded systems, network monitoring and control software, and test and development equipment.*