SpaceWire Router IP Core

SpaceWire is a data-handling network for use on-board spacecraft, which connects instruments, mass memory, processors, downlink telemetry, and other on-board sub-systems. SpaceWire has some specific characteristics that help it support data-handling applications in space.

STAR-Dundee offers essential SpaceWire interface and network components as VHDL IP blocks for use in FPGAs and ASICs. Our IP has proven to be robust and is widely used across the space industry, having been integrated into many FPGAs and flight ASICs.

Each of our SpaceWire IP cores has the following features:

- Delivered as synthesisable VHDL source code in obfuscated or clear code format
- Configurable, giving flexibility through generics in the VHDL source
- Easily targeted for major FPGAs including Microchip, AMD Xilinx, Altera, Lattice, and NanoXplore. Support for radiation tolerant device features.

Reference designs are available for AMD Xilinx and Microchip devices. Please contact STAR-Dundee for other target devices.

SpaceWire Router IP

The STAR-Dundee SpaceWire Router IP core is a SpaceWire routing switch which fully implements the network layer routing functions defined in the ECSS-E-ST-50-12C Rev.1 SpaceWire standard.

Functions

An overview of the functions and interfaces of the IP core is shown in the following figure.
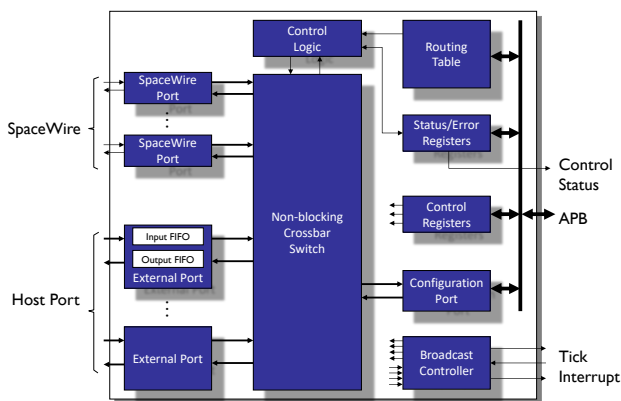
The IP core comprises a number of serial SpaceWire interfaces or optional parallel host port FIFO interfaces which are interconnected via a non-blocking wormhole packet switch. The packet switch implements address decoding for both path and logical address, output port arbitration, and packet routing.

A configurable logical address table provides support for logical addressing with two levels of priority, header deletion and group adaptive routing.

Each port has a watchdog timer function which can be used to recover blocked network paths.

Features

The STAR-Dundee SpaceWire Router IP permits the creation of a flexible wormhole router based on a non-blocking crossbar switch. The IP has the following features:

- Up to 31 ports, configured as SpaceWire or host ports
- Non-blocking fully connected switch
- Broadcast code distribution controller supporting SpaceWire time-code, and distributed interrupt codes without acknowledgement
- Ports can be set to start automatically when packets are ready to send and stop when there is no data to send
- Internal RMAP configuration port with APB register access option
- Logical address table with group adaptive routing option and scrubbing interface.
- Internal status/error registers accessible via the configuration port or APB
- APB master interface supporting system configuration.

Device Utilisation

The approximate utilisation figures for a typical SpaceWire Routing Switch implementation, including EDAC protected memories where available, are provided in the table below. AMD Xilinx FPGA results are obtained using XST or Vivado Synthesis. Microchip and Lattice results are obtained using Synplify synthesis. NanoXplore results are generated in Impulse.

Technology	Ports	LUT	FF	RAM
AMD Xilinx 7-Series	16	21576	14022	51[1]
AMD Xilinx UltraScale/UltraScale+	16	21011	14286	51[1]
AMD Xilinx Versal	16	17582	14411	51[1]
Microchip RTG4	8	15730	8639	18
Microchip PolarFire	16	34249	16130	17
Microchip RT PolarFire (TMR enabled)	16	52888	42380	17
NanoXplore NG-Ultra	16	27374	15149	17
Lattice CertusPro-NX	8	14373	7065	9

(1) Internal FIFOs are generated using AMD Xilinx XPM_FIFO EDAC protected primitives

Licensing

STAR-Dundee SpaceWire IP is available under license, provided as complete VHDL source code.

For more information on the IP cores, licensing, or if you have specific or custom requirements, please contact us.